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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
LEUNG, QUYEN PHAN	

ART UNIT	PAPER NUMBER
2828	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/964,463	ONOMURA ET AL.
	Examiner	Art Unit
	Quyen P. Leung	2828

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,7,9-12,14-18,20,21,23,24,26 and 28-31* is/are rejected.

7)☒ Claim(s) *4,6,8,22,25 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

As agreed upon during the interview of 8/4/2004, a new action is provided below.

Claims 1-12 and 14-31 are pending.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 11, 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 11, it is not clear how the sapphire substrate can have a first conductive type, because sapphire is insulating and does not conduct as would a first conductive type GaN substrate. Regarding claim 26, the range "0.05<=y<=0.02" is unclear and should be replaced with "0.05<=y<=0.20".

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2, 9, 11-12, 14, 15, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Sasanuma et al (JP 11-251685, see English language equivalent

USP 6252894 which will be referred to hereinafter). Sasanuma et al discloses the claimed invention. Figure 11 illustrates a semiconductor laser diode

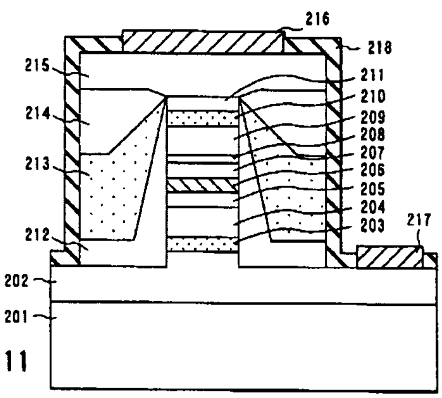

FIG. 11

[Sixth Embodiment]

FIG. **11** is a cross sectional view showing the schematic structure of a blue semiconductor laser according to a sixth embodiment of this invention.

As shown in FIG. **11**, on a sapphire substrate **201**, an n-GaN contact layer (Si doped: 5×10^{18} cm^{-3}, 3 μm) **202**, n-$In_{0.2}Ga_{0.8}N$ optical absorption layer (Si doped: 5×10^{18} cm^{-3}, 0.1 μm) **203**, n-$Al_{0.08}Ga_{0.92}N$ clad layer (Si doped: 1×10^{18} cm^{-3}, 0.8 μm) **204**, n-GaN optical guided layer (Si doped: 1×10^{18} cm^{-3}, 0.1 μm) **205**, multiple quantum well (MQW) active layer **206** including an $In_{0.15}Ga_{0.85}N$ well layer (3 nm, five layered) and $In_{0.02}Ga_{0.98}N$ barrier layer (6 nm), p-$Al_{0.2}Ga_{0.8}N$ carrier overflow preventing layer (20 nm) **207**, p-GaN optical guided layer (Mg doped: 1×10^{18} cm^{-3}, 0.1 μm) **208**, p-$Al_{0.08}Ga_{0.92}N$ clad layer (Mg doped: 1×10^{18} cm^{-3}, 0.8 μm) **209**, p-$In_{0.2}Ga_{0.8}N$ optical absorption layer (Mg doped: 5×10^{18} cm^{-3}, 0.1 μm) **210** and p-GaN contact layer (Mg doped: 2×10^{18} cm^{-3}, 0.1 μm) **211** are sequentially grown and formed.

A portion ranging from the surface of the p-type contact layer **211** to the intermediate portion of the n-type contact layer **202** is removed with a mesa portion left behind in a

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stripe form, and a p-$Al_{0.08}Ga_{0.92}N$ current block layer (Mg doped: 1×10^{18} cm^{-3}, 0.1 μm) **212**, n-$In_{0.2}Ga_{0.8}N$ optical absorption layer (Si doped: 5×10^{18} cm^{-3}, 0.3 μm) **213** and n-GaN current block layer (Si doped: 1×10^{18} cm^{-3}, 2 μm) **214** are grown and formed on the side wall of the mesa portion left behind. A p-GaN contact layer (Mg doped: 2×10^{18} cm^{-3}, 0.2 μm) **215** is grown and formed on the mesa portion and n-type current block layer **214**.

A portion ranging from the surface of the p-type contact layer **215** to the p-type current block layer **212** is partly removed, an n-side electrode (contact metallization) **217** formed of Al/Ti/Au is formed on the exposed surface of the n-type contact layer **202**, and a p-side electrode (contact metallization) **216** formed of Pt/Ti/Pt/Au is formed on the p-type contact layer **215**. An SiO_2 insulating film **218** is formed to cover an exposed portion on which the electrodes **216, 217** are not formed. The width of the MQW active layer **206** is set to 4 μm. Further, although not shown in the drawing, a highly reflective coat formed of multiple laminated layers of TiO_2/SiO_2 is formed on the laser light emission end surface.

comprising a contact layer made of GaN (202), a first conductive type nitride semiconductor layer (204) formed on the contact layer (202) and made of $Al_xGa_{1-x}N$ (0.04<=x<=0.08); a first conductive type clad layer (205) formed on the first conductive nitride semiconductor layer and made of nitride semiconductor; a core area (206)

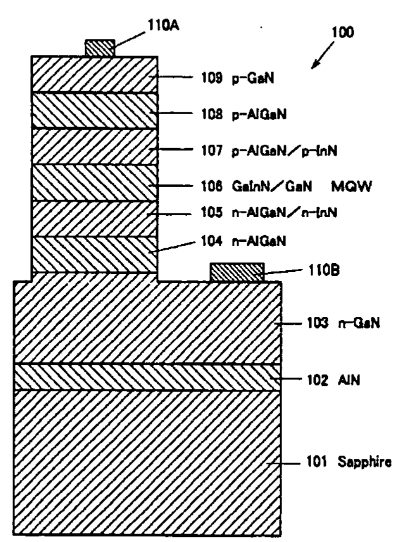
formed on the first conductive type clad layer (205) and made of nitride semiconductor, the core area (206) including an active layer to emit light by electric current injection; a second conductive type clad layer (208).

It is inherent that layer (205,208) are clad layers because they sandwich the core area as disclosed and claimed by applicant and further the materials of the clad layers (205,208) have a higher bandgap energy and lower refractive index as compared with the core region.

It is noted Sasanuma et al's figure 11 is a fair reading on the claimed invention, because (a) applicant did not claim that the first conductive type nitride semiconductor layer is <u>directly</u> on the contact layer and (b) applicant used open-ended claim terminology of "comprising" which allows for intervening layer 203.

5. Claims 1-2, 11-12, 14-15, and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Tezen et al(6,631,149). Tezen et al discloses the claimed invention of semiconductor laser device comprising a contact layer made of GaN (103), a first conductive type nitride semiconductor layer (104) formed on the contact layer (103) and made of $Al_xGa_{1-x}N$ (0.04<=x<=0.08); a first conductive type clad layer (105) formed on the first conductive nitride semiconductor layer and made of nitride semiconductor; a core area (106) formed on the first conductive type clad layer (105) and made of

FIG. 1



nitride semiconductor, the core area (106) including an active layer to emit light by electric current injection; a second conductive type clad layer (107).

It is inherent that layer (105,107) are clad layers because they sandwich the core area as disclosed and claimed by applicant and further the materials of the clad layers (105,107) have a higher bandgap energy and lower refractive index as compared with the core region.

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The invention will be more fully understood by reference to the following embodiment, but not limited thereto.

FIG. 1 illustrates a sectional view of a laser diode **100**. The laser diode **100** has a sapphire substrate **101** on which about 50 nm in thickness of buffer layer **102** comprising, for example, AlN is formed.

About 5 μm in thickness of silicon (Si) doped GaN n-layer **103**, having an electron concentration of $2\times10^{18}/cm^3$, is formed on the buffer layer **102**. About 1 μm in thickness of silicon (Si) doped $Al_{0.08}Ga_{0.92}N$ n-cladding layer **104**, having an electron concentration of $2\times10^{18}/cm^3$, is formed on the n-layer **103**. About 100 nm in thickness of n-guide layer **105**, having a multiple layer structure, is formed on the n-cladding layer **104**. As shown in FIG. **2** the n-guide layer **105** comprises five pairs of layers. Each pair comprises a silicon (Si) doped $Al_{0.01}Ga_{0.99}N$ layer having a thickness of 10 nm and an electron concentration of $2\times10^{18}/cm^3$ and a silicon (Si) doped InN layer having a thickness of 10 nm and an electron concentration of $2\times10^{18}/cm^3$, laminated alternately.

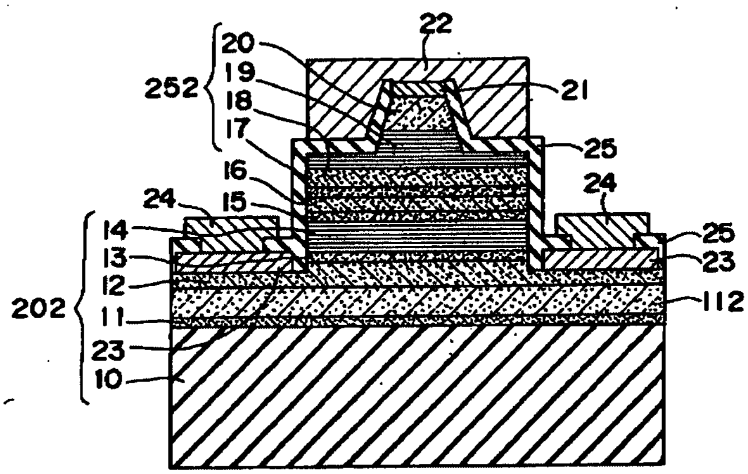
An active layer **106** having a multiple quantum well (MQW) structure is formed on the n-guide layer **105**. In the active layer **106**, 4 well layers made of $Ga_{0.85}In_{0.15}N$, each having a thickness of about 3 nm, and three barrier layers made of GaN, each having a thickness of about 5 nm, are laminated alternately as shown in FIG. **3**. About 100 nm in thickness of p-guide layer **107**, having a multiple layer structure, is formed on the active layer **106**. As shown in FIG. **4** the p-guide layer **107** comprises five pairs of layers. Each pair includes a magnesium (Mg) doped $Al_{0.01}Ga_{0.99}N$ layer, having a hole concentration of $5\times10^{17}/cm^3$ and a thickness of about 10 nm, and a magnesium (Mg) doped InN layer, having a hole concentration of $5\times10^{17}/cm^3$ and a thickness of about 10 nm.

About 1 μm in thickness of magnesium (Mg) doped $Al_{0.08}Ga_{0.92}N$ p-cladding layer **108**, having a hole concentration of $5\times10^{17}/cm^3$, is formed on the p-guide layer **107**. A magnesium (Mg) doped GaN p-contact layer **109**, having a thickness of 300 nm and a hole concentration of $5\times10^{17}/cm^3$, is formed on the p-contact layer **109**. An electrode layer **110A** made of nickel (Ni) is formed on some portion of the p-contact layer **109**. Another electrode **110B** made of aluminum (Al) is formed on some portion of the n-layer **103**.

6. Claims 1, 3, 5, 7, 9-12, 14-18, 20-21, 23-24, 26, and 28-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Nagahama et al (EP 1 017 113 A1). Nagahama et al discloses the claimed invention. Note together example 2, embodiment 2 and

figure 2, because Embodiment 2 (i.e. pages 12-17) and figure 2

Fig. 2



teach a sapphire substrate (10, see [0092], [0096]),

[0092] Fig. 2 is a schematic cross sectional view (cross section perpendicular to the direction of propagation of laser light) showing the configuration of a nitride semiconductor device according to the second embodiment of the present invention. The nitride semiconductor device is, for example, a nitride semiconductor laser diode device which has an active layer 16 comprising a nitride semiconductor interposed by a semiconductor region 202 of n conductivity side (consisting of an n-side contact layer 12, a crack preventing layer 13, an n-side cladding layer 14 and an n-side optical waveguide layer 15) and a semiconductor region 252 of p conductivity side (consisting of a cap layer 17, a p-side optical waveguide layer 18, a p-side cladding layer 19 and a p-side contact layer 20) provided on a C plane of a substrate 10 made of sapphire or the like.

[0096] The substrate 10 may be made of, in addition to sapphire having principal plane in C plane, sapphire having principal plane in R plane or A plane, insulating substrate such as spinel ($MgAl_2O_4$), or other semiconductor substrate such as SiC (including 6H, 4H and 3C), ZnS, ZnO, GaAs and GaN.

a GaN layer (11, see [0097]),

[0097] The buffer layer 11 is formed by growing AlN, GaN, AlGaN, InGaN, etc., for example, at a temperature within 900°C to a thickness of several tens to several hundreds of angstroms. While the buffer layer 11 is formed for the purpose of relaxing lattice constant mismatch between the substrate and the nitride semiconductor, it may be omitted depending on the method of growing the nitride semiconductor, type of substrate and other conditions.

a first conductive nitride semiconductor layer (12, see [0101-0103], [0219]),

[0101] The n-side contact layer 12 acts as a contact layer whereon a negative electrode is formed, of which thickness is preferably controlled within a range from 0.2 μm to 4 μm. When the thickness is less than 0.2 μm, it becomes difficult to control the etching rate for exposing the layer in a subsequent process of forming the negative electrode. When the thickness is greater than 4 μm, on the other hand, quality of crystal tend to become poorer due to impurity. The n-side contact layer 12 is made of, for example, GaN doped with Si. Doping concentration of n-type impurity in the nitride semiconductor of the n-side contact layer 12 is preferably in a range from $1 \times 10^{17}/cm^3$ to $1 \times 10^{21}/cm^3$, and more preferably from $1 \times 10^{18}/cm^3$ to $1 \times 10^{19}/cm^3$. When the concentration is lower than $1 \times 10^{17}/cm^3$, satisfactory ohmic contact with the n electrode material cannot be obtained and therefore threshold current and voltage cannot be decreased in a laser device. When the concentration is higher than $1 \times 10^{21}/cm^3$, leak current in the device increases and the quality of crystal deteriorate, resulting in a shorter device life. It is desirable to set the impurity concentration in the n-side contact layer 12 higher than that of the n-cladding layer 14 thereby to increase the carrier concentration in the n-side contact layer 12, in order to reduce the ohmic contact resistance with the n electrode 23. When an electrically conductive substrate such as GaN, SiC, ZnO or the like is used as the substrate and the negative electrode is installed on the back of the substrate, the n-side contact layer 12 acts as a buffer layer, not as a contact layer.

[0102] At least one of the second buffer layer 11 and the n-side contact layer 12 may also be made in super lattice structure, in which case quality of crystal of the layer are drastically improved and the threshold current can be decreased. Preferably the n-side contact layer 12 which is thinner than the second buffer layer 11 is made in super lattice structure. When the n-side contact layer 12 is made in such a super lattice structure that the first layer and the second layer having different levels of band gap energy are laminated, contact resistance with the n electrode 23 can be decreased and the value of threshold can be decreased by exposing the layer having lower band gap energy thereby to form the n electrode 23. As materials to make the n electrode 23 for providing favorable ohmic contact with the n-type nitride semiconductor, there are metals such as Al, Ti, W, Si, Zn, Sn and In, and alloys thereof.

[0103] When the n-side contact layer 12 is made in super lattice structure of different impurity concentration, resistance in the transverse direction can be reduced due to an effect similar to that of HEMT described in conjunction with the first embodiment, thereby making it possible to reduce the threshold voltage and current of the LD device.

Example 2

[0219] With the same procedure as in Example 1, for the n-side contact layer 12, a 30-angstrom-thick first layer consisting of n-type $Al_{0.05}Ga_{0.95}N$ doped with Si to $2 \times 10^{19}/cm^3$ was grown and subsequently, a 30-angstrom-thick second layer consisting of undoped GaN was grown and these procedures were repeated, resulting in superlattices having a total thickness of 1.2 μm. The other constructions of the laser devices were the same as in Example 1. The threshold current density was $2.7kA/cm^2$, the threshold voltage was 4.2V and the lifetime was 60 hours or longer.

a first type cladding nitride layer (14, see [0105]),

[0105] The n-side cladding layer is made of n-type $Al_{0.2}Ga_{0.8}N$ doped with Si in a concentration of $5 \times 10^{18}/cm^3$ in super lattice structure made by laminating the first layer 20 angstroms thick and the second layer made of undoped GaN 20 angstroms thick alternately, and has an overall thickness of, for example, 0.5 μm. The n-side cladding layer 14 functions as a carrier trapping layer and light trapping layer and, when it is made in super lattice structure, one of the layers is preferably made by growing a nitride semiconductor which includes Al, preferably AlGaN. When the layer is grown to a thickness not less than 100 angstroms and within 2 μm, more preferably in a range from 500 angstroms to 1 μm, a good carrier trapping layer can be formed. While the n-side cladding layer 14 may be made by growing a single nitride semiconductor, it may also be made in a super lattice layer which enables it to form a carrier trapping layer of good quality of crystal without cracks.

a core (16, see [0107]),

[0107] The active layer 16 is made by alternately laminating a quantum well layer which is made of, for example, $In_{0.2}Ga_{0.8}N$ doped with Si in a concentration of $8 \times 10^{18}/cm^3$ and has a thickness of 25 angstroms and a barrier layer made of $In_{0.05}Ga_{0.95}N$ doped with Si in a concentration of $8 \times 10^{18}/cm^3$ and has a thickness of 50 angstroms, thereby forming a layer of multiple quantum well structure (MQW) having a specified thickness. In the active layer 16, either both or one of the quantum well layer and the barrier layer may be doped with the impurity. When doped with an n-type impurity, threshold value tends to decrease. When the active layer 16 is made in multiple quantum well structure as described above, it is always formed by laminating the quantum well layer having a lower band gap energy and a barrier layer having a band gap energy lower than that of the quantum well layer, and is therefore distinguished from super lattice layer. Thickness of the quantum well layer is within 100 angstroms, preferably within 70 angstroms and most preferably 50 angstroms. Thickness of the barrier layer is within 150 angstroms, preferably within 100 angstroms and most preferably 70 angstroms. For example, the quantum well structure active layer disclosed by Japanese Non-examined Patent Publication No. 9-148678 (U.S. Patent Application 08/743,72).

and a second type clad nitride layer (19, see [0111]).

[0111] The p-side, cladding layer 19 is made of p-type $Al_{0.2}Ga_{0.8}N$ doped with Mg in a concentration of $1 \times 10^{20}/cm^3$ in super lattice structure made by alternately laminating the first layer 20 angstroms thick and the second layer which is made of p-type GaN and is doped with Mg in a concentration of $1 \times 10^{20}/cm^3$ having a thickness of 20 angstroms. The p-side cladding layer 19 functions as a carrier trapping layer similarly to the n-side cladding layer 14 and particularly functions as a layer for decreasing the resistivity of the p-type layer. While limits of thickness of the p-side cladding layer 19 are not specified, too, it is preferably formed to a thickness not less than 100 angstroms and not greater than 2 _m, more preferably not less than 500 angstroms and not greater than 1 μm.

Attention is directed to paragraph [0103]

[0103] When the n-side contact layer 12 is made in super lattice structure of different impurity concentration, resistance in the transverse direction can be reduced due to an effect similar to that of HEMT described in conjunction with the first embodiment, thereby making it possible to reduce the threshold voltage and current of the LD device.

which teaches that layer (12) can be made of super lattice structure for reducing the threshold voltage and current of the LD device, and to example 2 (or paragraph [0219])

Example 2

[0219] With the same procedure as in Example 1, for the n-side contact layer 12, a 30-angstrom-thick first layer consisting of n-type $Al_{0.05}Ga_{0.95}N$ doped with Si to $2 \times 10^{19}/cm^3$ was grown and subsequently, a 30-angstrom-thick second layer consisting of undoped GaN was grown and these procedures were repeated, resulting in superlattices having a total thickness of 1.2 μm. The other constructions of the laser devices were the same as in Example 1. The threshold current density was $2.7kA/cm^2$, the threshold voltage was 4.2V and the lifetime was 60 hours or longer.

which teaches a particular super lattice structure for layer (12) of figure 2, including a layer having the composition of $Al_xGa_{1-x}N$ layer where $0.04<=x<=0.8$.

Regarding independent claims 21, 24, note [0101] which states in the last line "when an electrically conductive substrate such as GaN,..., is used as the substrate and the negative electrode is installed on the back of the substrate, the n-side contact layer acts as a buffer layer, no as a contact layer."

[0101] The n-side contact layer 12 acts as a contact layer whereon a negative electrode is formed, of which thickness is preferably controlled within a range from 0.2 μm to 4 μm. When the thickness is less than 0.2 μm, it becomes difficult to control the etching rate for exposing the layer in a subsequent process of forming the negative electrode. When the thickness is greater than 4 μm, on the other hand, quality of crystal tend to become poorer due to impurity. The n-side contact layer 12 is made of, for example, GaN doped with Si. Doping concentration of n-type impurity in the nitride semiconductor of the n-side contact layer 12 is preferably in a range from $1 \times 10^{17}/cm^3$ to $1 \times 10^{21}/cm^3$, and more preferably from $1 \times 10^{18}/cm^3$ to $1 \times 10^{19}/cm^3$. When the concentration is lower than $1 \times 10^{17}/cm^3$, satisfactory ohmic contact with the n electrode material cannot be obtained and therefore threshold current and voltage cannot be decreased in a laser device. When the concentration is higher than $1 \times 10^{21}/cm^3$, leak current in the device increases and the quality of crystal deteriorate, resulting in a shorter device life. It is desirable to set the impurity concentration in the n-side contact layer 12 higher than that of the n-cladding layer 14 thereby to increase the carrier concentration in the n-side contact layer 12, in order to reduce the ohmic contact resistance with the n electrode 23. When an electrically conductive substrate such as GaN, SiC, ZnO or the like is used as the substrate and the negative electrode is installed on the back of the substrate, the n-side contact layer 12 acts as a buffer layer, not as a contact layer.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quyen P. Leung whose telephone number is (571)272-1943. The examiner can normally be reached on 8-4:30, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571)272-1835. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quyen P. Leung
Primary Examiner
Art Unit 2828

QPL